Refine Search

Search Results -

Terms	Documents
L4 and (PCI or "PCI Express")	54

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, June 11, 2007 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB; PLUR=YES; OP=OR			
L5	L4 and (PCI or "PCI Express")	54	L5
L4	l2 same (mode or type or phase)	588	L4
L3	L2 and (PCI or "PCI Express")	249	L3
L2	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	2332	L2
DB=DWPI; PLUR=YES; OP=OR			
L1	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	250	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L7 and (PCI or "PCI Express")	123

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L8

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, June 11, 2007 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L8	L7 and (PCI or "PCI Express")	123	L8
L7	l6 same (mode or type or phase)	9329	L7
L6	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	25620	L6
DB=PGPB; PLUR=YES; OP=OR			
L5	L4 and (PCI or "PCI Express")	54	L5
L4	l2 same (mode or type or phase)	588	L4
L3	L2 and (PCI or "PCI Express")	249	L3
L2	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	2332	L2
DB=DWPI; PLUR=YES; OP=OR			
L1	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	250	L1

Refine Search

Search Results -

Terms	Documents
L8 and L9	5

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L10

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, June 11, 2007 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name results
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L10	l8 and L9	5	L1
L9	710/100,33,300-302,72,306,313;345/520,531;361/679,683,783;709/253;326/37;375/376;370/254.ccls.	17257	L9
L8	L7 and (PCI or "PCI Express")	123	L8
L7	l6 same (mode or type or phase)	9329	L7
L6	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	25620	L6
	DB=PGPB; PLUR=YES; OP=OR		
L5	L4 and (PCI or "PCI Express")	54	L5
L4	l2 same (mode or type or phase)	588	L4
L3	L2 and (PCI or "PCI Express")	249	L3
L2	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	2332	L2

DB=DWPI; PLUR=YES; OP=OR

L1	(port near10 connect$4) same (set or bunch or group) same (less or smaller or "same")	250	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L3	308

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, June 11, 2007 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	l1 and L3	308	L4
L3	L2 and (card or board or motherboard)	30455	L3
L2	(port near10 connect$4) same (mode or type or phase)	106141	L2
L1	710/14,106,107,305,311;370/351.ccls.	5686	L1

END OF SEARCH HISTORY

Results for "((port<in>metadata) <and> (connect*<in>metadata))<and> (set<in>..." e-mail
Your search matched **1** of **1585504** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

((port<in>metadata) <and> (connect*<in>metadata))<and> (set<in>metadata) a Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **HiBRID-SoC: a system-on-chip architecture with two multimedia DSPs an**
Friebe, L.; Stolberg, H.-J.; Berekovic, M.; Moch, S.; Kulaczewski, M.B.; Dehnh
R.;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip]
17-20 Sept. 2003 Page(s):85 - 88
AbstractPlus | Full Text: PDF(461 KB) IEEE CNF
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HiBRID-SoC: a system-on-chip architecture with two multimedia DSPs and a RISC core

Friebe, L. Stolberg, H.-J. Berekovic, M. Moch, S. Kulaczewski, M.B. Dehnhardt, A. Pirsch, R.
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Abstract
The HiBRID-SoC integrates three fully programmable processor cores, each optimized towards a particular class of algorithm: the HiPAR-DSP for DSP oriented functions, the macroblock processor for block oriented algorithms, and the stream processor for bitstream processing. Dedicated interface units for SDRAM, serial Flash, and host system access are **connected** via a 64 bit AMBA AHB system bus with the processor cores. Dual-**port** memories between the processor cores facilitate fast data and control information exchange between the cores. The HiBRID-SoC is fabricated in a 0.18 /spl mu/m 6LM standard-cell technology, occupies about 82 mm/sup 2/, and operates at 160 MHz.

Index Terms

Inspec

Controlled Indexing

digital signal processing chips integrated circuit design logic design multimedia computing reduced instruction **set** computing system buses system-on-chip

Non-controlled Indexing

0.18 micron 160 MHz 64 bit ARB system bus interface DSP oriented functions HiBRID-SoC RISC core SDRAM SoC bitstream processing block oriented algorithms control information exchange data information exchange dual-**port** memories fully programmable processor cores host system access macroblock processor multimedia DSP multimedia signal processing applications serial Flash stream processor system-on-chip architecture

Author Keywords
Not Available